

The documentation and process conversion measures necessary to comply with this revision shall be completed by 8 August 2003.

INCH-POUND

MIL-PRF-19500/675B
8 May 2003
SUPERSEDING
MIL-PRF-19500/675A
30 August 2001

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED (TOTAL DOSE AND SINGLE EVENT EFFECTS) TRANSISTORS, N-CHANNEL, SILICON TYPES 2N7463T2 AND 2N7464T2 AND U5 SUFFIXES JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and Single Event Effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (EAS) and maximum avalanche current (IAS).

1.2 Physical dimensions. See figure 1 (TO-205AF, T2 suffix) and figure 2 (LCC, U5 suffix).

* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$ (free air)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (2) (3) $T_C = +25^\circ\text{C}$	I_{D2} $T_C = +100^\circ\text{C}$	I_S (2)	I_{DM} (4)	T_{op} and T_{STG}	VISO 70,000 foot altitude
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>°C</u>	<u>V dc</u>
2N7463T2, 2N7463U5	25	0.8	400	400	± 20	2.9	1.9	3.0	12	-55 to	400
2N7464T2, 2N7464U5	25	0.8	500	500	± 20	2.5	1.6	2.6	10.4	+150	500

(1) Derate linearly $0.2 \text{ W}/^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.

(2) The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires:

$$I_D = \sqrt{\frac{T_J \text{ max} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{Jmax})}}$$

(3) See figure 3, maximum drain current graph.

(4) $I_{DM} = 4 \times I_{D1}$ as calculated in note (2).

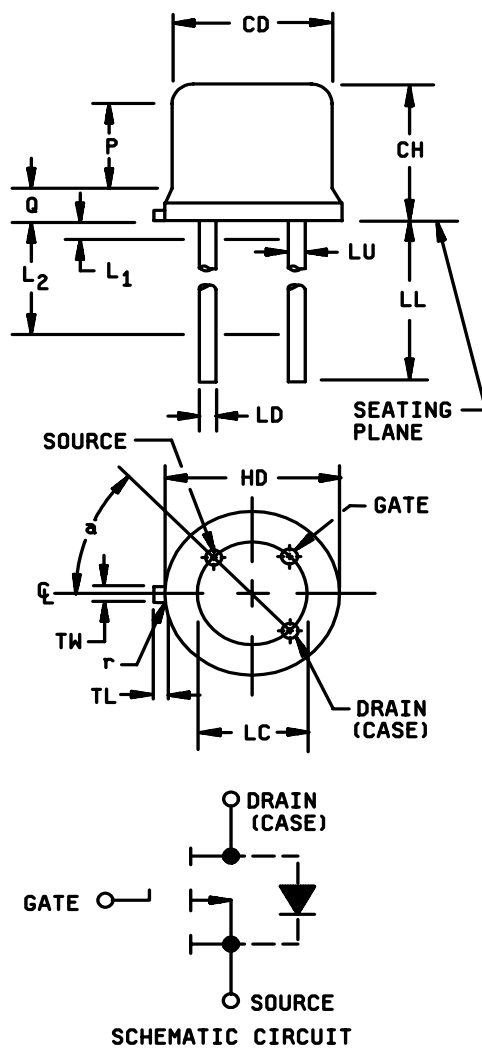
Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC/VAC, Post Office Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5961

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Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
CD	.315	.355	8.00	9.02
CH	.160	.180	4.06	4.57
HD	.340	.370	8.64	9.40
LC	.200 BSC		5.08 BSC	
LD	.016	.021	0.41	0.53
LL	.500	.750	12.70	19.05
LU	.016	.019	0.41	0.48
L1		.050		1.27
L2	.250		6.35	
P	.070		1.78	
Q		.050		1.27
r	.009	.041	0.23	1.04
TL	.029	.045	0.74	1.14
TW	.028	.034	0.71	0.86
a	45°			

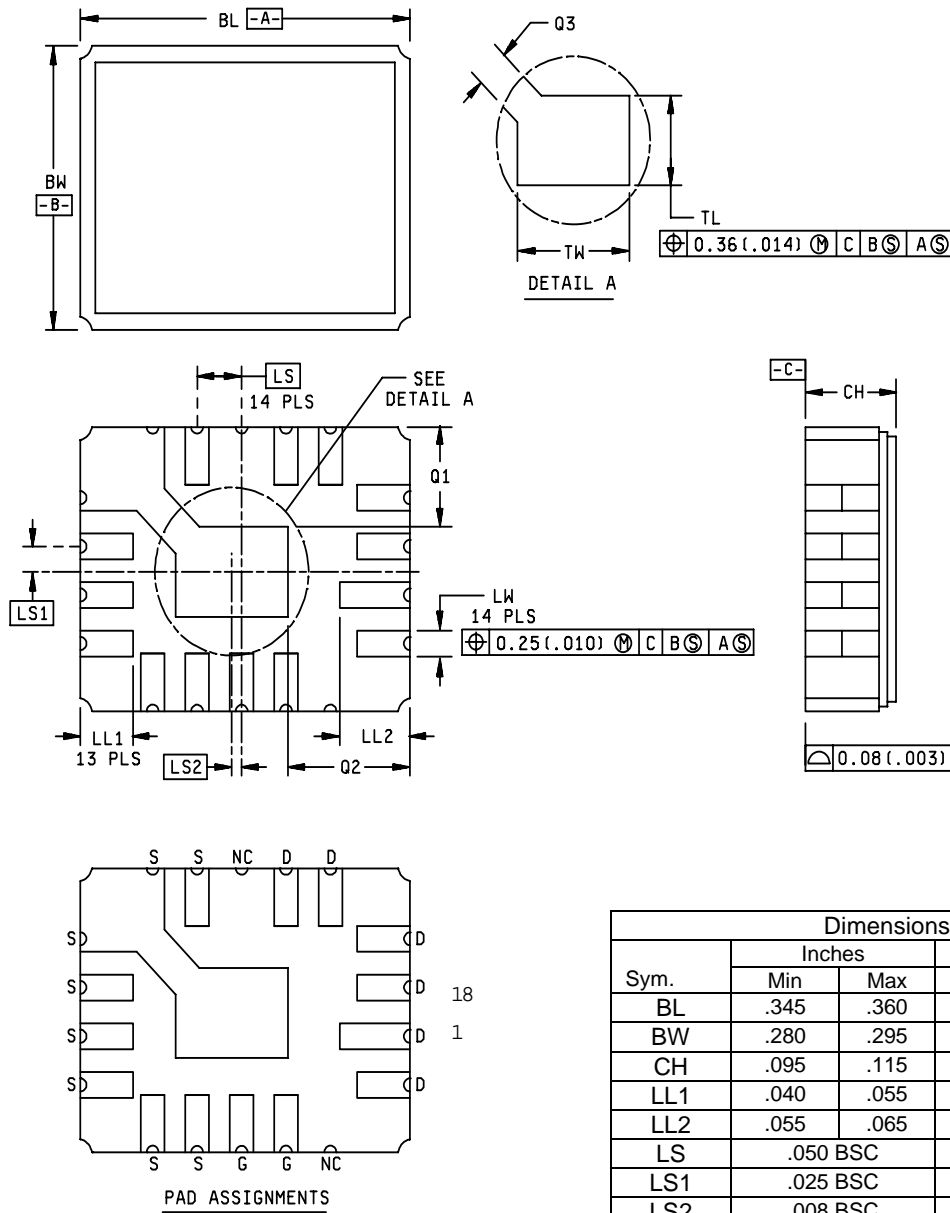


NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Lead number 1 is the source, lead number 2 is the gate, lead number 4 is omitted from this outline. The drain is number 3 and is electrically connected to the case.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Physical dimensions for TO-205AF (2N7463T2 and 2N7464T2).

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NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 2. Physical dimensions for LCC (2N7463U5 and 2N7464U5).

* 1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 1.0 mA dc	V _{GS(TH)} V _{DS} ≥ V _{GS} I _D = 1.0 mA dc	Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(ON)} (1) V _{GS} = 12 V dc		R _{θJC} max	E _{AS} at I _{D1}	I _{AS}	
				T _J = +25°C at I _{D2}	T _J = +150°C at I _{D2}				
2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	V dc	V dc		μA dc	ohm	ohm	°C/W	mJ	A
		Min	Max						
	400	2.5	4.5	50	1.39	3.0	5.0	140	3.0
500	2.5	4.5	50	1.77	3.9	5.0	148	2.6	

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS} - Rated avalanche current, non-repetitive.

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (TO-205AF, T2 suffix) and 2 (LCC, U5 suffix) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

* 3.7 Electrical test requirements. The electrical test requirements shall be table I as specified herein.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.2.1 Group E inspection. Group E inspection shall be conducted in accordance with MIL-PRF-19500 and table III herein. End-point electrical measurements shall be in accordance with the applicable tests of table I, subgroup 2 herein.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. Figure 4 illustrates the design safe operation area. End-point measurements shall be in accordance with table III.

* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with MIL-PRF-19500 (table IV), and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.1)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.1)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.2)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.2)
(3)	Gate stress test (see 4.3.3)	Gate stress test (see 4.3.3)
(3) 9	Subgroup 2 of table I herein; I_{GSSF1} , I_{GSSR1} , I_{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$ $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value	Subgroups 2 and 3 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value

- (1) At the end of the test program, I_{GSSF} and I_{GSSR} are measured.
- (2) An out-of-family program to characterize I_{GSSF} and I_{GSSR} shall be invoked.
- (3) Shall be performed anytime before screen 10.

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* 4.3.1 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS}) $I_{AS(max)}$.
- b. Peak gate voltage (V_{GS})- 12 V.
- c. Gate to source resistor (R_{GS}) $25\Omega \leq R_{GS} \leq 200\Omega$.
- d. Initial case temperature (T_C) $+25^\circ\text{C} +10^\circ\text{C}, -5^\circ\text{C}$.
- e. Inductance (L) $\left[\frac{2E_{AS}}{(I_{DI})^2} \right] \left[\frac{(V_{BR} - V_{DD})}{V_{BR}} \right] \text{ mH minimum .}$
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 50 V.

* 4.3.2 Thermal impedance ($Z_{\theta JC}$ measurements). The $Z_{\theta JC}$ measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit (not to exceed figure 5, thermal impedance curves and the table I, subgroup 2 limits) for $Z_{\theta JC}$ in screening (table IV of MIL-PRF-19500) shall be derived by each vendor by means of statistical process control. When the process has exhibited control and capability, the capability data shall be used to establish the fixed screening limit. In addition to screening, once a fixed limit has been established, monitor all future sealing lots using a random five piece sample from each lot to be plotted on the applicable \bar{X} , R chart. If a lot exhibits an out of control condition, the entire lot shall be removed from the line and held for engineering evaluation and disposition. This procedure may be used in lieu of an in line procedure.

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H) 1 A minimum (1.3 A minimum for LCC).
- c. Heating time (t_H) 10 ms.
- d. Drain-source heating voltage (V_H)-..... 25 V (15 V for LCC).
- e. Measurement time delay (t_{MD}) 30 μs to 60 μs .
- f. Sample window time (t_{SW}) 10 μs maximum.

* 4.3.3 Gate stress test. Apply $V_{GS} = 30 \text{ V}$ minimum for $t = 250 \mu\text{s}$ minimum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Alternate flow is allowed for quality conformance inspection in accordance with MIL-PRF-19500.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JANTX and JANTXV) of MIL-PRF-19500, and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

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4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2037	Test condition A, all internal wires for each device shall be pulled separately.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Test condition D, 2,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 30 seconds minimum.
B5	1042	Test condition B, $V_{GS} = \text{rated}$ $T_A = +175^{\circ}\text{C}$, $t = 24$ hours.
B5	1042	Test condition A, $V_{DS} = \text{rated}$; $T_A = +175^{\circ}\text{C}$; $t = 120$ hours.
B5	2037	Not applicable.
B6	3161	Not applicable.

4.4.2.2 Group B inspection, table VIb (JANTX and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening)
B3	1042	Test condition D, 2,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 30 seconds minimum.
B3	2037	Test condition A. All internal bond wires for each device shall be pulled separately.
B4	2075	See 3.4.2.
B4	2077	Not applicable.
B5 and B6		Not applicable.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with the applicable of table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	1056	Test condition B.
C2	2036	Test condition E (applicable to T0 - 205AF only).
C2	1021	Omit initial conditioning.
C5	3161	See 4.5.2.
C6	1042	Test condition D, 6,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 30 seconds minimum.
C6	2037	Test condition A. All internal bond wires for each device shall be pulled separately. (Wire bond pull test performed if devices continued from group B).
C7	1018	No pre-bake required.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC(max)} = 5.0^{\circ}\text{C/W}$. The following parameter measurements shall apply:

- a. Measuring current (I_M)10 mA.
- b. Drain heating current (I_H)1 A (1.3 A minimum for LCC).
- c. Heating time (t_H)Steady-state (see method 3161 of MIL-STD-750 for definition).
- d. Drain-source heating voltage (V_H)25 V (15 V for LCC).
- e. Measurement time delay (t_{MD})30 μs to 60 μs .
- f. Sample window time (t_{SW})10 μs maximum.

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* TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3161	See 4.3.2	$Z_{\theta JC}$		1.40	$^{\circ}\text{C/W}$
Breakdown voltage, drain to source 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3407	$V_{GS} = 0 \text{ V dc}$, $I_D = 1 \text{ mA dc}$, bias condition C	$V_{(BR)DSS}$	400 500		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	2.5	4.5	V dc
Gate current	3411	$V_{GS} = +20 \text{ V dc}$ and -20 V dc , bias condition C, $V_{DS} = 0$	I_{GSS1}		± 100	nA dc
Drain current	3413	$V_{GS} = 0 \text{ V dc}$, bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS1}		50	$\mu\text{A dc}$
Static drain to source on-state resistance 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$		1.39 1.77	Ω Ω
Static drain to source on-state resistance 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(on)2}$		1.52 1.9	Ω Ω
Forward voltage 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$, $V_{GS} = 0 \text{ V dc}$	V_{SD}		1.2 1.2	V V

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High-temperature operation:		T _C = T _J = +125°C				
Gate current	3411	V _{GS} = +20 V dc and -20 V dc, bias condition C, V _{DS} = 0	I _{GSS2}		±200	nA dc
Drain current	3413	V _{GS} = 0 V dc, bias condition C, V _{DS} = 100 percent of rated V _{DS}	I _{DSS2}		1.0	mA dc
Drain current	3413	V _{GS} = 0 V dc, bias condition C, V _{DS} = 80 percent of rated V _{DS}	I _{DSS3}		0.25	mA dc
Static drain to source on-state resistance 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3421	V _{GS} = 12 V dc, pulsed (see 4.5.1), I _D = I _{D2}	r _{DS(on)3}		2.64 3.76	Ω Ω
Gate to source voltage (thresholds)	3403	V _{DS} ≥ V _{GS} , I _D = 1 mA dc	V _{GS(TH)2}	1.5		V dc
Low-temperature operation:		T _C = T _J = -55°C				
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = 1 mA dc	V _{GS(TH)3}		5.5	V dc
<u>Subgroup 4</u>						
Forward transconductance 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3475	I _D = rated I _{D2} , V _{DD} = 15 V (see 4.5.1)	g _{FS}	0.5 0.4		S S
Switching time test	3472	I _D = I _{D1} , V _{GS} = 12 V dc, R _G = 7.5Ω, V _{DD} = 50 percent of rated V _{DS}				
Turn-on delay time 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5			t _{d(on)}		35 35	ns ns

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit		
	Method	Conditions		Min	Max			
<u>Subgroup 4</u> - Continued								
Rise time 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3474	See figures 6 and 7; t _p = 10 ms V _{DS} = 200 V See table I, subgroup 2 herein.	t _r		78 60	ns ns		
Turn-off delay time 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5			t _{d(off)}		65 67	ns ns		
Fall time 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5			t _f		66 52	ns ns		
<u>Subgroup 5</u>								
Safe operating area (SOA) test (high voltage)			3471	Condition B	Q _{G(on)}		31 30	nC nC
Electrical measurements								
<u>Subgroup 6</u>								
Not applicable								
<u>Subgroup 7</u>								
Gate charge On-state gate charge 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5			3471	Condition B	Q _{GS}		8.5 8	nC nC
Gate to source charge 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5								

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> - Continued						
Gate to drain charge			Q_{GD}			
2N7463T2, 2N7463U5					20	nC
2N7464T2, 2N7464U5					18	nC
Reverse recovery time	3473	$dI/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 50 \text{ V}$, $I_D = I_{D1}$	t_{rr}			
2N7463T2, 2N7463U5					350	ns
2N7464T2, 2N7464U5					400	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test is required for the following end-point measurements only (not intended for screen 13): Group B, subgroups 3 and 4 (JANS) or group B, subgroups 2 and 3 (JANTXV); group C, subgroup 6; group E, subgroup 1.

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* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
<u>Subgroup 1</u>								
Not applicable								
<u>Subgroup 2</u>		T _C = +25°C						
Steady-state total dose irradiation (V _{GS} bias) <u>4/</u>	1019	V _{GS} = 12V V _{DS} = 0						
Steady-state total dose irradiation (V _{DS} bias) <u>4/</u>	1019	V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)						
End-point electricals		See table I, subgroup 2 herein.						
Breakdown voltage, drain to source	3407	Bias condition C V _{GS} = 0 I _D = 1 mA	V _{(BR)DSS}					
2N7463T2, 2N7463U5 2N7464T2, 2N7464U5				400 500		400 500		V dc V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS}	V _{Gsth1}					
2N7463T2, 2N7463U5 2N7464T2, 2N7464U5				2.5 2.5	4.5 4.5	2.0 2.0	4.5 4.5	V dc V dc
Gate current	3411	Bias condition C V _{GS} = 20 V V _{DS} = 0	I _{GSSF1}		100		100	nA dc
Gate current	3411	Bias condition C V _{GS} = -20 V V _{DS} = 0	I _{GSSR1}		-100		-100	nA dc
Drain current	3413	Bias condition C V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)	I _{DSS1}		50		50	μA dc

See footnotes at end of table.

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* TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
Static drain to source on-state voltage 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	3405	V _{GS} = 12 V condition A pulsed (see 4.5.1) I _D = I _{D2}	V _{DSon1}		2.641 2.832		2.641 2.832	V dc V dc
Forward voltage source to drain diode 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	4011	V _{GS} = 0 I _D = I _{D1}	V _{SD}		1.2 1.2		1.2 1.2	V dc V dc

1/ For sampling plan, see MIL-PRF-19500.

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			12 devices c = 0
Thermal shock (temperature cycling)	1051	Test condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			12 devices c = 0
Steady-state reverse bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 3</u>			3 devices c = 0
DPA	2102		
<u>Subgroup 4</u>			sample size N/A
Thermal resistance, thermal impedance curves	3161	Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
<u>Subgroup 5</u>			15 devices c = 0
Reduced barometric pressure	1001	$V_{DS} = \text{rated } V_{(BR)DSS}, I_{(ISO)} < 0.25 \text{ mA}$	
<u>Subgroup 6</u>			3 devices
ESD	1020		
Electrical measurements		See table I, subgroup 2	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only. - Continued

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 7</u> SEE <u>2/ 3/ 4/</u> Electrical measurements <u>5/</u> SEE irradiation 2N7463T2, 2N7463U5 2N7464T2, 2N7464U5 Electrical measurements <u>2/</u>	1080	I_{GSS1} and I_{DSS1} in accordance with table I, subgroup 2 Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec Temperature = $+25 \pm 5^{\circ}C$ LET = 28 MeV-cm ² /mg Range = 43 microns Energy = 285 MeV Insitu bias conditions: $V_{DS} = 325V$ & $V_{GS} = -15V$ LET = 37 MeV-cm ² /mg Range = 39 microns Energy = 305 MeV Insitu bias conditions: $V_{DS} = 325V$ & $V_{GS} = -10V$ $V_{DS} = 275V$ & $V_{GS} = -15V$ LET = 28 MeV-cm ² /mg Range = 43 microns Energy = 285 MeV Insitu bias conditions: $V_{DS} = 375V$ & $V_{GS} = -20V$ LET = 37 MeV-cm ² /mg Range = 39 microns Energy = 305 MeV Insitu bias conditions: $V_{DS} = 350V$ & $V_{GS} = -10V$ $V_{DS} = 325V$ & $V_{GS} = -15V$ $V_{DS} = 300V$ & $V_{GS} = -20V$ I_{GSS1} and I_{DSS1} in accordance with table I, subgroup 2	3 devices
<u>Subgroup 8</u> Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		22 devices, c = 0

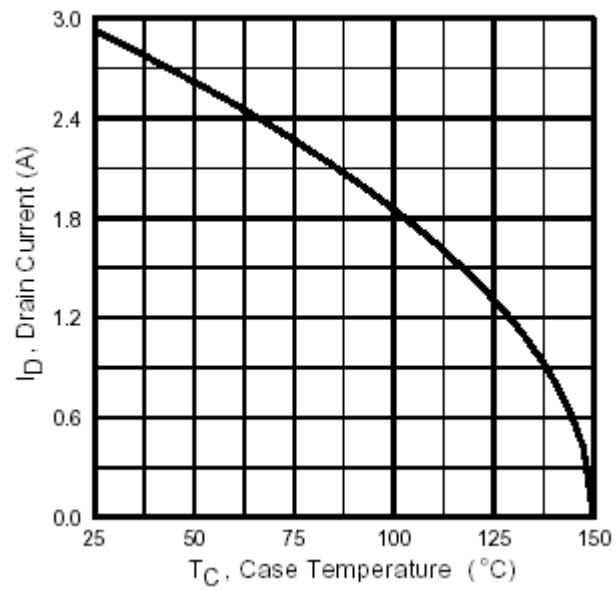
1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other performance specifications utilizing the same structurally identical die design.

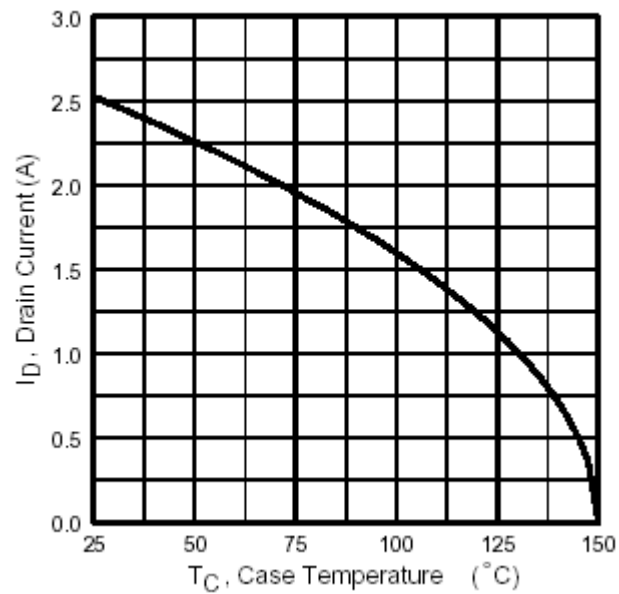
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LET's.

4/ The sampling plan applies to each bias condition.

5/ Examine I_{GSS1} and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

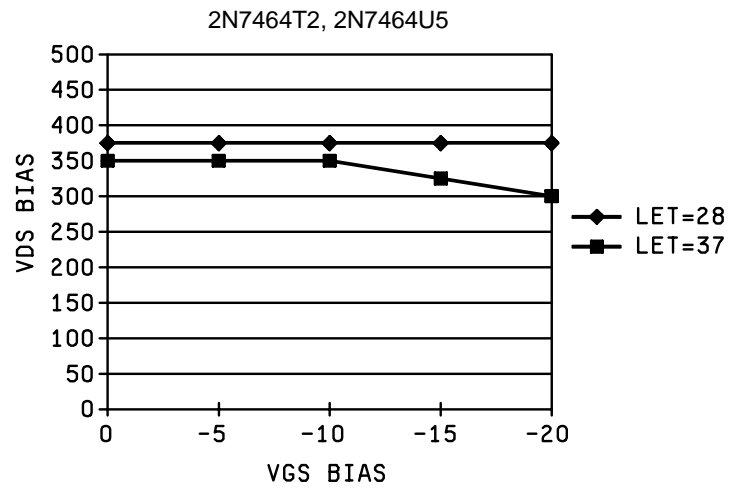
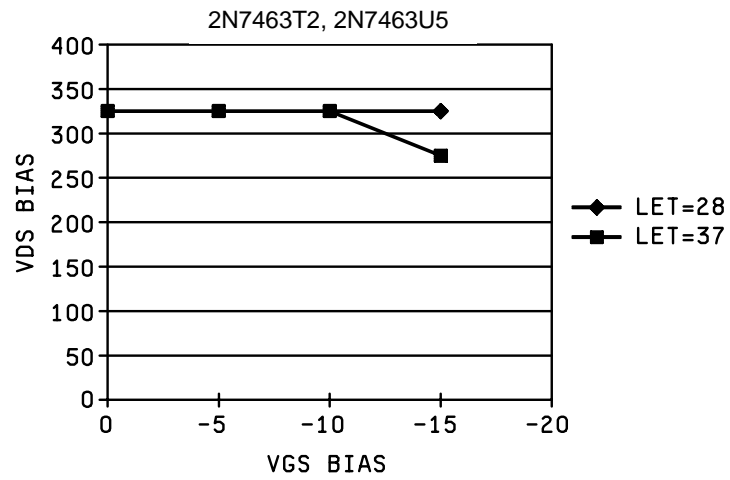


2N7463T2, U5



2N7464T2, U5

* FIGURE 3 Maximum drain current vs case temperature.



* FIGURE 4. SEE SOA graph.

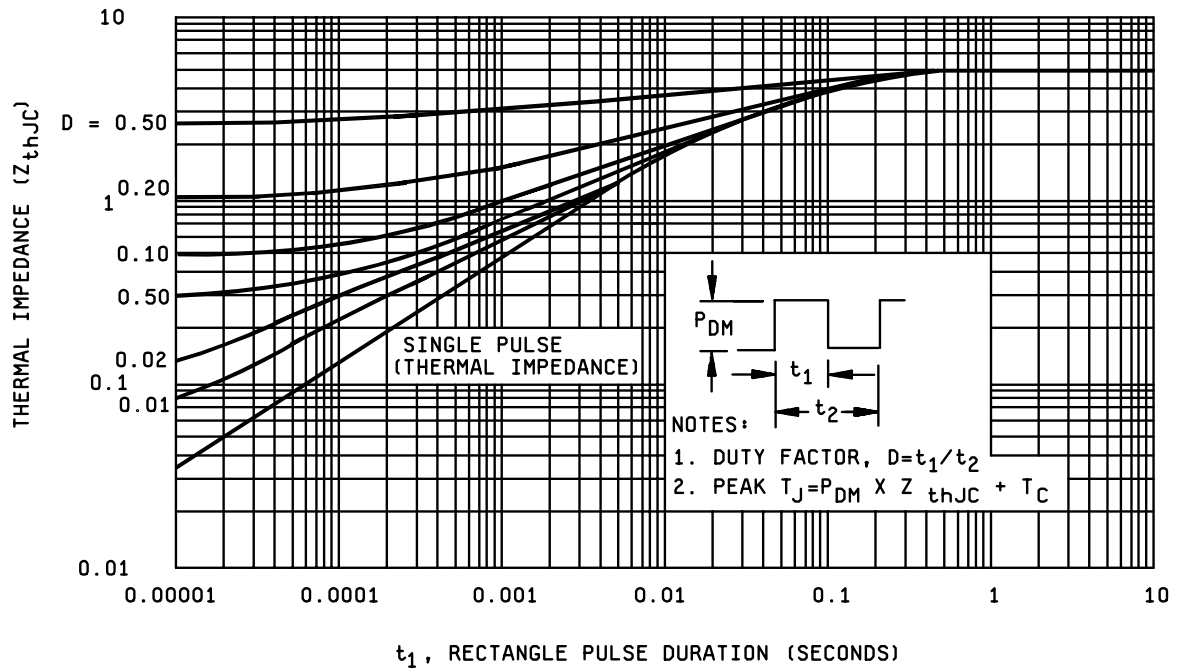
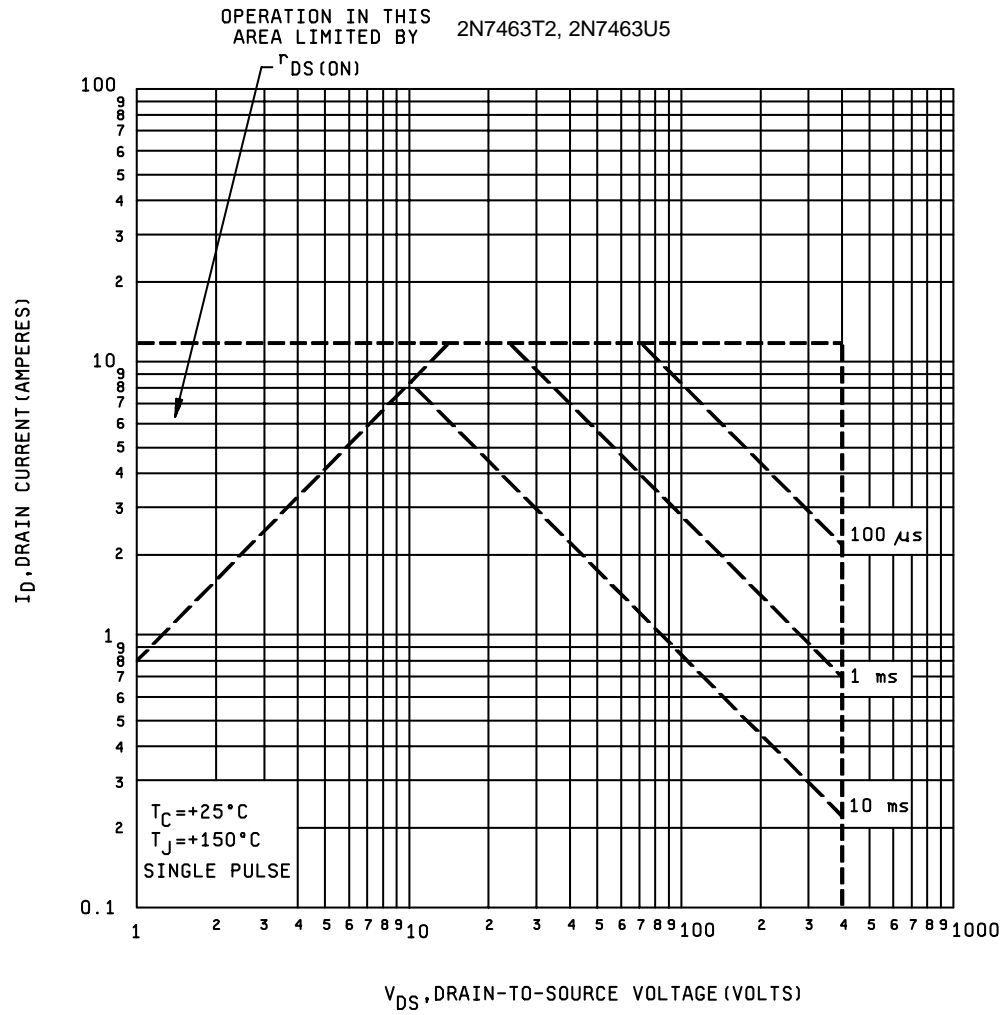
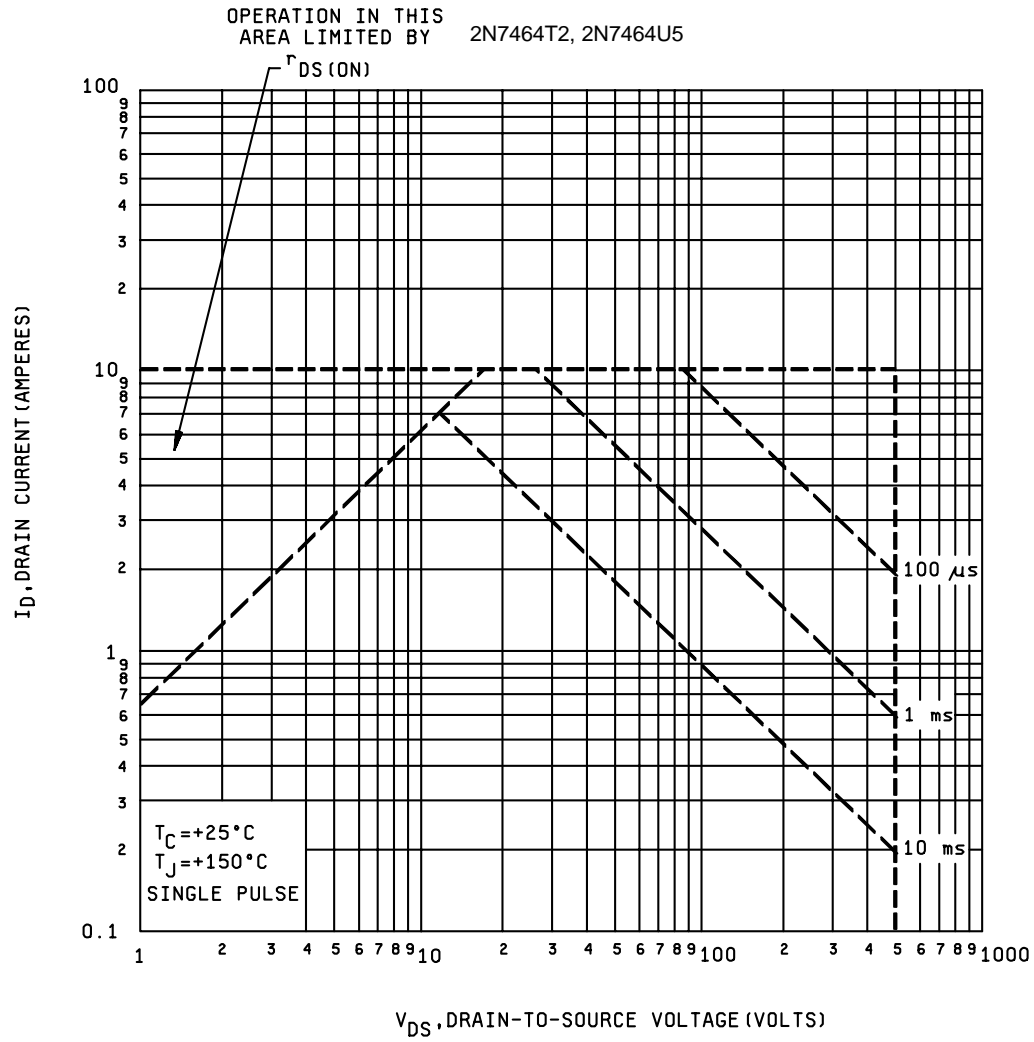


FIGURE 5. Thermal impedance curves.



* FIGURE 6. SOA graph.



* FIGURE 7. SOA graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification.
- b. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.2.1).
- c. Packaging requirements (see 5.1).
- d. Lead finish (see 3.4.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000.

* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types	Commercial types	
	TO-205AF	LCC
2N7463T2, 2N7463U5 2N7464T2, 2N7464U5	IRHF7330SE IRHF7430SE	IRHE7330SE IRHE7430SE

* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2718)

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I RECOMMEND A CHANGE:

1. DOCUMENT NUMBER
MIL-PRF-19500/675B

2. DOCUMENT DATE
8 May 2003

3. **DOCUMENT TITLE** SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED (TOTAL DOSE AND SINGLE EVENT EFFECTS) TRANSISTORS, N-CHANNEL, SILICON TYPES 2N7463T2 AND 2N7464T2 AND U5 SUFFIXES JANTXVR AND JANSR

4. **NATURE OF CHANGE** (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. **REASON FOR RECOMMENDATION**

6. SUBMITTER

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b. ORGANIZATION

c. ADDRESS (Include Zip Code)

d. TELEPHONE (Include Area Code)
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DSN
FAX
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7. DATE SUBMITTED

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